COLOR FILTER CONFIGURATION FOR A SILICON WAFER TO BE DICED INTO PHOTOSENSITIVE CHIPS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is a divisional of U.S. Application No. 09/802,792 filed 03/08/2001 by the same inventors, and claims priority therefrom.

[0002] Cross-reference is hereby made to the following co-pending US Patent Application, assigned to the assignee hereof: "Systems and Methods for Fabricating an Electro-Optical Device Used for Image Sensing," Serial No. 09/750,425, Filed December 28, 2000 (Attorney Docket Nos. D/A0707 or XXT-092).

TECHNICAL FIELD

[0003] The present invention relates to photosensitive chips for creating electrical signals from an original image, as would be found, for example, in a digital scanner or facsimile machine. More specifically, the present invention relates to a design for a photosensitive chip with a thin-film color filter attached thereto.

BACKGROUND

[0004] As copying and scanning of color hard-copy documents becomes more prevalent in the business world, there has arisen a need for full-color solid-state photosensitive devices, such as a silicon chip having an array of photosensors thereon. One prior-art for causing the photosensors on the silicon chip to be sensitive to a specific primary color is to provide, on the main surface of the silicon chip, a layer of spectrally transparent filter material, such as polyimide or acrylic, which has been dyed or pigmented to a specific primary color. If a single

photosensitive chip is intended to have multiple linear arrays of photosensors, each linear array being sensitive to one particular primary color, particular polyimide layers are applied to specific linear arrays, thereby creating a full-color photosensitive chip.

[0005] One typical method of construction of full-color photosensitive chip is to first create a wafer having a relatively large number, such as one hundred or more, of semiconductor structures, each structure corresponding to one chip. Filters are applied to the structures on the wafer so that filter areas will be applied to the desired linear arrays of photosensors on each chip structure. Typically this application of filter material is carried out by applying an even layer of translucent liquid to the entire wafer, developing the desired areas of the filter material with a photo mask, and then etching away the translucent material in all other areas. For full-color chips, multiple layers of translucent filter material are applied to the wafer, and then etched away as needed, to yield the three primary-color-filtered linear arrays of photosensors. Only after the filter layers are applied as desired is the wafer "diced," or sawed into individual chips. According to one technique, the chip termination is a combination of chemically-etched v-groove and a mechanically sawed portion. The diced chips are first tested and screened for defective chips, and the usable chips are then abutted into a longer linear array.

[0006] In the construction of full-color photosensitive chips having translucent filter layers attached thereto, certain practical problems are evident. One problem concerns the inadvertent ripping or other damage to the cured filter layers when the wafer is diced into individual chips: the relatively thin translucent filter layer, particularly at the photosensors toward either end of the chip, can be torn by the action of a saw blade. If the translucent color filter is torn in a manner that even a very small portion (as little as 1%) of the area of one photosite is exposed to unfiltered white light, this extra light thus introduced to the photosite will have an appreciable effect on resulting image quality. It is therefore crucial that the translucent filters be placed on a wafer from which chips are created such that the integrity of the filters is maintained throughout the manufacturing process.

PRIOR ART

[0007] U.S. Patent 5,219,796 discloses the basic concept of dicing image sensor chips from a wafer.

[0008] U.S. Patent 5,521,125 discloses a technique of dicing silicon chips from a wafer. "Streets" of relatively deep trenches are formed between the functional chip areas of the wafer, and a shock absorbent material is a deposited in the streets, forming a concave meniscus therein. The shock absorbent material retards the trajectories of silicon particles set into motion when the wafer is diced into chips.

[0009] U.S. Patent 5,604,362 discloses covering essentially the entire main surface of a photosensor chip with a highly light-absorbing filter layer, to avoid stray reflections from non-photosite portions of a photosensor chip.

[0010] U.S. Patent 5,696,626 discloses the design of a photosensitive chip wherein each photosite is covered with a filter formed from a cured translucent liquid. At the critical ends of the chip, between the end photosite and the edge of the chip, there is provided a ridge which protrudes over the regular thickness of the filter. This ridge maintains the physical integrity of the filter, particularly during a dicing process.

[0011] U.S. Patent 6,111,247 discloses an imaging chip having a sensor portion and a non-sensor portion disposed about the periphery of the sensor portion, a passivation layer overlying a portion of a top surface of the sensor portion, and a protection layer overlying the passivation layer.

[0012] U.S. Patent 6,066,883 discloses using a "guard ring," in the form of a biased diffusion area, to avoid the influence of stray light in an edge photosite in a photosensor chip.

[0013] U.S. Patent 6,157,019 discloses a configuration of photosensitive chips in which photosites immediately adjacent a functional edge of the chip are shielded and thus defined with an opaque layer that overlaps the diced region and preserves the integrity of the filter layers while eliminating the need for a guard ring.

SUMMARY

[0014] According to one aspect of the present invention, there is provided a photosensitive chip for use in an imaging apparatus, comprising a main surface, having at least one photosite thereon, the main surface defining an edge. A groove portion is defined at the edge. A light-transmissive planar layer is disposed over the main surface, the planar layer forming a planar surface substantially parallel with the main surface, the planar layer extending over the groove portion. A light-transmissive filtering layer is disposed over the planar layer.

[0015] According to another aspect of the present invention, there is provided an imaging apparatus including at least one photosensitive chip. The chip comprises a main surface, having at least one photosite thereon, the main surface defining an edge. A groove portion is defined at the edge. A light-transmissive planar layer is disposed over the main surface, the planar layer forming a planar surface substantially parallel with the main surface, the planar layer extending over the groove portion.

[0016] According to another aspect of the present invention, there is provided an integrated circuit wafer, comprising a first chip area defined in a main surface of the wafer, the first chip area including structure related to a first photosite. A groove is defined in the wafer, the groove defining at least one edge of the first chip area. A light-transmissive planar layer is disposed over the main surface, the planar layer forming a planar surface substantially parallel with the main surface, the planar layer extending over the groove.

[0017] According to another aspect of the present invention, there is provided a method of making photosensitive chips for use in an imaging apparatus, comprising the steps of providing an integrated circuit wafer, the wafer comprising a first chip area defined in a main surface of the wafer, the first chip area including structure related to a first photosite, and a groove defined in the wafer, the groove defining at least one edge of the first chip area, and providing a light-transmissive planar layer

over the main surface, the planar layer forming a planar surface substantially parallel with the main surface, the planar layer extending over the groove.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Figure 1 is a plan view of a single photosensitive chip of a general design found, for example, in a full-color photosensor scanner.

[0019] Figure 2 is a perspective view of a wafer from which chips may be diced pursuant to the present invention.

[0020] Figure 3 is a detailed cross-sectional view showing the internal structure of a chip according to the present invention, along with a filter architecture pursuant to the present invention.

[0021] Figure 4 is a plan view showing the configuration of various translucent filtering layers over a chip when the chip is attached to an adjacent chip within a wafer pursuant to the present invention.

[0022] Figure 5 is an elevational view of a portion of a photosensitive device including chips made pursuant to the present invention.

DETAILED DESCRIPTION

[0023] Figure 1 is a plan view of a single photosensitive chip, generally indicated as 10, of a design found, for example, in a full-color photosensor scanner or digital camera. A typical design of a full-page-width scanner will include a plurality of chips 10, each chip being approximately one-half to one inch in length, the chips being butted end-to-end to form an effective collinear array of photosensors, which extends across a page image being scanned. Each chip 10 is a silicon-based integrated circuit chip having defined in a main surface thereof three independently-functioning linear arrays of photosensors, each photosensor being here indicated as 14. The photosensors are disposed in three parallel rows which extend across a

main dimension of the chip 10, these individual rows being shown as 16A, 16B, and 16C. Each individual row of photosensors on chip 10 can be made sensitive to a particular color, by applying to the particular row a spectrally translucent filter layer which covers only the photosensors in a particular row. In a preferred embodiment of the present invention, the three rows of photosensors are each filtered with a different primary color, such as red, green, and blue. Generally, each individual photosensor 14 is adapted to output a charge or voltage signal indicative to the intensity of light of a certain type impinging thereon; various structures, such as transfer circuits, or charge-coupled devices, are known in the art for processing signal output by the various photosensors corresponding to photosites 14.

[0024] Figure 2 is a perspective view of a wafer 100, generally of an integrated circuit design familiar in the art, from which any number of chips 10 may be separated or "diced." A basic description of the dicing process is given, for instance, in US Patents 5,219,796 or 5,696,626, cited above. (The wafer is indicated as "prior art" in Figure 2 only to the extent that dicing photosensitive chips from a wafer is known; however, aspects of the invention may be embodied in such a wafer 100, such as shown in Figure 4.)

[0025] The view shown in Figure 3 corresponds to the cross-section through line marked 3-3 in Figure 2, in the case where a particular chip 10 is still formed as part of a wafer, from which it and any number of other chips are diced. In the illustrated embodiment, there is provided a ridge 20 which protrudes from the main surface of the chip, and is disposed to extend between the perimeter of an end photosite 14 disposed at the end of a particular chip 10, and the edge of the chip, as shown in Figure 2. This ridge 20 protrudes a significant distance from the main surface of the chip, typically about 0.8 to 1.2 micrometers from the surface formed by the end photosite 14.

[0026] With regard to the specific internal structure of a chip 10 in the illustrated embodiment, all of the interconnect layers on the chip 10 are formed on a

field oxide indicated as 50, the specific structure of which is not germane to the present invention. Above this field oxide is a borophosphosilicon glass, indicated as 52. There is also a metal structure 54, which is typically made of aluminum, first and second layers 56 and 58 of inter-metal oxide, and further a light shield indicated as 60. The topmost layer of both ridge 20 and the neighboring structures on the chip is a top oxide layer here indicated as 62. Also shown in this particular embodiment are doped implants 64 and 66: implant 64 is an optional guardring structure useful in some chip designs, while 66 forms part of a "doughnut" structure familiar in some designs of CMOS photosensors.

[0027] When chips such as 10 are still part of an original wafer, as shown in Figure 3, in this embodiment of the invention the portions of the wafer corresponding to individual chips are separated by a relatively deep groove 70, which can be an etched V-groove, as shown, or alternately some other trench-like structure. Dimensionally, groove 70 should be wide enough to accommodate the edge placement variation of the dicing blade which separates the chip areas into chips: a typical location of the edge of the portion of the wafer removed by a dicing blade is shown as line 71. Once again, a basic description of the dicing process is given, for instance, in US Patents 5,219,796 and 5,696,626, cited above.

[0028] With particular reference to the present invention, there is further shown in Figure 3 the structure of light-transmissive filter layers which are placed over the wafer forming a plurality of chips 10. As shown, a planar layer 72 is placed over the entire structure and allowed to fill groove 70 and cover ridge 20, yielding a substantially planar surface generally parallel to the main surface of chip 10. Over this planar surface is placed a filtering layer 74. Both planar layer 72 and filtering layer 74 are preferably made of a relatively brittle or glassy material, such as acrylic, which is placed over the chip 10 in a liquid form and allowed to harden or dry by various means known in the art.

[0029] Different requirements of an imaging apparatus will mandate that respective layers 72, 74 have various light-transmitting properties, such as transparency, translucence, opacity, etc., with respect to any or all wavelengths. In one practical embodiment of the invention, planar layer 72 is substantially transmissive of all visible wavelengths of light, and filtering layer 74 is transmissive of only a portion of the visible spectrum. In an apparatus for recording visible light, different types of filtering layers 74, transmitting different portions of the spectrum, can be used to create a photosensor chip, such as shown in Figure 1, in which each row 16A, 16B, 16C of photosites can be made sensitive to one primary color.

[0030] Figure 4 is a plan view showing the configuration of various types of filtering layers 74 over a chip 10 and an adjacent chip 10' within a wafer. In this particular embodiment, there is provided a relatively short "scribe area" 75 of otherwise unused wafer area between chips 10 and 10', and successive blade cuts are used to cut through the respective grooves 70 and 70', as described, for example, in U.S. Patent 5,219,796. As shown, in this view there are provided three distinct filtering layers, indicated as 74A, 74B, and 74C, which respectively cover rows of photosites 14 described above as 16A, 16B, and 16C. Typically, the three types of filters 74 will each transmit only one primary color, red, green, or blue, so that the chip 10 itself can output image data reflective of the entire visible spectrum, as is familiar in the art. Significantly, as shown in the Figure, the respective areas covered by filters 74A, 74B, and 74C each extend over one linear array, i.e., row 16 of photosites 14; and the same filter area such as 74A for one chip 10 extends across the groove 70, scribe area 75, another groove 70', and over the equivalent row such as 16A for the adjacent chip 10'. Indeed, if there are a number of chips 10 in a row along one dimension in a wafer, each filtered area should extend across the suitable row 16 of photosites for as many chips 10 as is geometrically possible. Once again, where a filter 74 extends over a groove 70, the filter 74 is disposed over and supported by a clear layer 72 (as shown in Figure 3) which presents a substantially planar surface over the groove 70.

[0031] The described configuration of filter layers 72 and 74 yields desirable practical results in the dicing process. When a wafer is diced, such as along a groove 70, the fact that each filter layer 74 is disposed over and supported by clear layer 72, which itself takes up most of the void formed by the groove 70, the filter layer 74 exhibits very little damage or tearing, especially in the portions thereof around any photosites 14. Also helpful is the use of acrylic-based material, the essential nature of which is known in the art, for layers 72 and 74. As mentioned above, the avoidance of disturbances to the filter layers 74 over the photosites is crucial to creation of a reliable photosensor chip 10.

[0032] Figure 5 is an elevational view showing relevant portions of an example photosensor device, such as could be used in conjunction with a digital copier or facsimile, using chips 10 made according to the present invention. Two chips 10 and 10' are disposed on a substrate 200. (Of course, in a full-page-width array of butted chips such as used, for example, in a digital copier or facsimile, there may be as many as twenty such chips arranged on a substrate.) The respective sets of photosites in each chip may be configured, such as by butting or spacing the chips closely together, to yield what is in effect a single functional array of photosites, as is familiar in the art. Each chip includes, at critical edges thereof, portions of grooves 70, as described above, which are remnants of the dicing process. Each chip further includes a layer 72 which, even in the finished chip, has the effect of creating a substantially planar surface of the portion of groove 70. The layer 72 is, in this embodiment, light-transmissive. Disposed over the planar surface of layer 72 is a light-transmissive layer 74, which may be a translucent color filter for at least one set of photosites on the chip.

[0033] The claims, as originally presented and as they may be amended, encompass variations, alternatives, modifications, improvements, equivalents, and substantial equivalents of the embodiments and teachings disclosed herein, including those that are presently unforeseen or unappreciated, and that, for example, may arise from applicants/patentees and others.